Remarks

Claims 1, 6-7, 10-12, 14-16, 17-38 and 44-46 are pending.

Rejections Based On Betsui

All pending claims stand rejected under Section 103 as being obvious over Miyamoto, Yoshizawa and the newly cited Betsui (5572041) (and other references for some of the claims).

Claims 1 and 10 -- Discrete Emission Region In Electron Source Layer.

Claim 1 has been amended to recite forming a first single crystal electron source layer on an underlying second single crystal electron source layer and defining a discrete emission region in the first single crystal electron source layer. Claim 10 has been amended to recite a single crystal electron source comprising an epitaxial layer formed on a single crystal support, the single crystal electron source including a discrete emission region. Support for these amendments may be found in Figs. 4(B)-4(D) (emission region 56) and in the Specification at page 7, lines 14-22.

Betsui Fig. 8 and the accompanying text at column 6, lines 47-63, teach an emitter device 10 constructed as a transistor 65. Betsui's transistor 65 includes a collector 66 formed on an n+ doped silicon substrate 14. (Part number 14 in Fig. 8 of Betsui points to collector layer 66. This does not appear to be correct. Rather, it seems clear from the descriptive text that part number 14 should point to the n+ substrate underlying collector layer 66. Betsui column 6, lines 50-53.) Betsui does not teach a discrete emission region in collector layer 66. Indeed, Betsui does not expressly teach any emission region in collector layer 66. Even if it is assumed that collector layer 66 is itself some kind of generalized emission region, Besui clearly does not teach a discrete emission region in layer 66. Furthermore, the use of the transistor 65 as the emitter device 10 in Betsui, with its narrowing base 68 and emitter 70, seems to make a discrete emitter region in collector layer 66 unnecessary. Hence, the claimed discrete emission region is neither inherent in nor suggested by Betsui. The same is true for Miyamoto which forms an emitter region in the conductor (not in the electron source) with a hole in an insulating layer interposed between the dielectric and the conductor.

Claims 1 and 10 and the claims depending from Claim 10, therefore, distinguish patentably over the combination of Miyamoto, Yoshizawa and Betsui.

Claims 6, 25 and 44 – Semiconductor Between Source And Dielectric.

Claim 6 recites forming an epitaxial semiconductor layer over a single crystal source and forming an epitaxial dielectric layer overlying the semiconductor layer. Claims 25 and 44 recite an epitaxial semi-conductor layer between the electron source and the epitaxial dielectric layer.

The Office asserts that the combination of Miyamoto, Yoshizawa and Betsui teaches the method of Claim 6 and the structure of each of Claims 25 and 44. The Office, however, does not address the above mentioned semiconductor layer in any of its remarks. In fact, none of the cited references teach or suggest this limitation.

The Office is directed to Fig. 2(D) for one example of a semiconductor layer (layer 28) between the source layer (layer 22) and the dielectric layer (layer 30). In each of Miyamoto, Yoshizawa and Betsui, the dielectric is formed on the electron source with no intervening semiconductor layer -- CaF_2 layer on n-Si layer in Miyamoto, insulator 13 on Si electron supply layer 12 in Yoshizawa and base 68 on collector 66 in Betsui. The cited references do not teach or suggest all of the elements of Claims 6, 25 and 44 and the rejection of those claims along with their respective dependent claims should be withdrawn.

The foregoing is believed to be a complete response to the outstanding Office Action.

Respectfully submitted,

/Steven R. Ormiston/

Steven R. Ormiston
Registration No. 35,974
(208) 433-1991 x204